Patent claims

1. A high-speed router for transmitting data packets, containing header data and useful data, between data networks, the router (1) having a plurality of data processing processors (12, 13, 14, 15) for parallel data processing of the header data.

2. The high-speed router as claimed in claim 1, wherein
a demultiplexer (6) is provided for separating the data packets present on the high-speed router (1) into header data and useful data.

3. The high-speed router as claimed in claim 1 or 2, wherein
a distribution processor (10) is provided for distributing the separated header data to the data processing processors (12, 13, 14, 15).

4. The high-speed router as claimed in one of the preceding claims,
wherein
the distribution processor (10) distributes the header data on the basis of the priority of the header data and the workload of the data processing processors (12, 13, 14, 15).

5. The high-speed router as claimed in one of the preceding claims,
wherein
the header data are distributed to the data processing processors (12, 13, 14, 15) by means of DMA operations.

6. The high-speed router as claimed in one of the preceding claims,
wherein

a CAM coprocessor (21) having an associative memory is provided for classifying the data packets.

7. The high-speed router as claimed in one of the preceding claims,
wherein
a useful data memory (9) is provided for buffer-storing the separated useful data.

8. The high-speed router as claimed in one of the preceding claims,
wherein
the header data and useful data in a data packet contain a respective identifier (ID).

9. The high-speed router as claimed in one of the preceding claims,
wherein
a first multiplexer (24) is provided for compiling header data and useful data, the useful data coming from the useful data memory (9) or from a switching mechanism.

10. The high-speed router as claimed in one of the preceding claims,
wherein
a second multiplexer (32) is provided for compiling the useful data buffer-stored in the useful data memory (9) and the header data.

11. The high-speed router as claimed in one of the preceding claims,
wherein
the first multiplexer (24) has a FIFO memory (29) connected downstream of it for outputting the compiled data packets through the router (1).

12. The high-speed router as claimed in one of the preceding claims,
wherein
the output of the second multiplexer (32) is connected to the switching mechanism.

13. The high-speed router as claimed in one of the preceding claims,
wherein
the distribution processor (10), the data processing processors (12, 13, 14, 15) and the CAM coprocessor (21) are connected to a common header data bus (7).

14. The high-speed router as claimed in one of the preceding claims,
wherein
each data processing processor (12, 13, 14, 15) is connected to a dedicated local memory (16, 17, 18, 19).

15. The high-speed router as claimed in one of the preceding claims,
wherein
a common memory (20) is additionally connected to the header data bus (7).

16. The high-speed router as claimed in one of the preceding claims,
wherein
the CAM coprocessor (21) is connected to the header data bus (7) via FIFO buffer memories (22, 23).

17. The high-speed router as claimed in one of the preceding claims,
wherein

the demultiplexer (6) has an input buffer (4) connected upstream of it.

18. The high-speed router as claimed in one of the preceding claims,
wherein
the data networks are LAN networks.

19. The high-speed router as claimed in one of the preceding claims 1-17,
wherein
one of the data networks is the Internet.

20. The high-speed router as claimed in one of the preceding claims,
wherein
the distribution processor (10) and the data processing processors (12, 13, 14, 15) are processors of the same processor type.